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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,594	05/16/2001	Toyohiko Yoshida	57454-116	9350

7590 05/11/2007

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

MAIL DATE	DELIVERY MODE
05/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/855,594	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 7-9* is/are pending in the application.

4a) Of the above claim(s) *3 and 11-18* is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 19* is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-9* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1,2,4-10,19 remain for examination. Claims 3,11-18 have been canceled.

2. Claims 1,2,4,5,7,8,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okado (EP 051 1484 A2) in view of Hennessy (Computer Architecture) in view of Dean (5,544,342).

3. As to the newly amended language "throughput" in claim 1, see discussion in response to applicant's remark below.

4. The rejections are maintained and incorporated by reference the last office action on 07/20/06.

5. The response foiled on 02/06/07 has been fully considered but is not persuasive.

6. In the remarks, applicant argued that:

a) Okado, Hennessy and Dean do not teach memory operation unit perform pipeline control having a same throughput and a different latency compared to the access to the instruction memory when accessing to the high speed instruction memory;

b) Okado, Hennessy and Dean do not teach the data memory and the integer operation unit are connected to the input and output bus to access the memory at the high speed.

7. As to a) above, Okado did not specifically show memory operation unit perform pipeline control having a same throughput and a different latency compared to the access to the instruction memory when accessing to the high speed instruction memory as clamed. However, However, Dean disclosed a memory operation unit (see dynamic pipeline cycle generating unit in fig.15) having a same throughput and different latency (faster) for generating pipeline cycles corresponding to the instruction readout from a high speed memory (see instruction cache for high speed instruction memory in fig, 15, see also col.25, lines 10-59). It would have been obvious to one of ordinary skill in the e art to include memory operation unit perform pipeline control having a same

throughput and a different latency compared to the access to the instruction memory when accessing to the high speed instruction memory because the use of Dean could provide Okado the ability to process the instruction from the high speed memory (e.g. the cache) at reduced instruction cycles, such as the fetch and decode, in a predetermined pipeline sequence, and because Okado did teach a repeat controller portion which allowed instructions to be read (fetched) from the micro ROM (instruction memory, see Col. 10, lines 12-15), which was a suggestion of the need for memory operating unit for generating the pipeline cycle in order to minimize the latency of the instruction fetch in the ROM, and for doing so, provided a motivation.

8. As to b), examiner holds that a data memory and an integer operation unit must be connected to the input and output bus, or the like, in order to access the memory at high speed. Otherwise, the high speed wouldn't be functional. One of ordinary skill in the art should be able to recognize the connections of I/O, for example, to the data memory and an integer unit at a given speed (high or low).

9. Claims 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the second bank select circuit decodes the address including the low order address to generate the chip select of the memory banks so diffident memory bank is accessed when data at the continuous addresses in the two different regions are accessed.

10. Claims 10,19 are allowable over the art of record for reciting the combined details of the instruction memory, data memory, instruction decoder, the register file, the memory operating unit, he integer unit, the retaining of the loop instructions, the generation of the pipeline cycles, the first flag indicating a first execution at the first execution cycle and retaining the fetched instruction in the register file when repeat instruction was executed, the second flag indicating second execution cycle to the last execution cycle at the second execution cycle to the last execution cycle and executed the loop while fetching the instruction retained in the dedicated register.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP